10. (Amended) A method of synthesizing a register transfer level (RTL) based design of a system comprising the steps of:

determining sub-modules of a top level system;

determining individual time budgets for each sub-module based on timing requirements of the top-level system

synthesizing gate-level designs of the sub-module based on the determined time budgets for the individual sub-modules;

integrating the gate-level designs of the individual sub-modules to form a top level design;

testing the top-level design for conformance with top-level design requirements;

generating gate-level netlists for the gate-level designs of each of the sub-modules; and

generating a top-level netlist when the top-level design conforms to the top-level design requirements.

IN THE ABSTRACT:

Please replace the existing Abstract with the new Abstract as attached on a separate sheet as follows: